FAIRCHILD SEMICONDUCTOR™

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ML4800

Power Factor Correction and PWM Controller Combo

Features

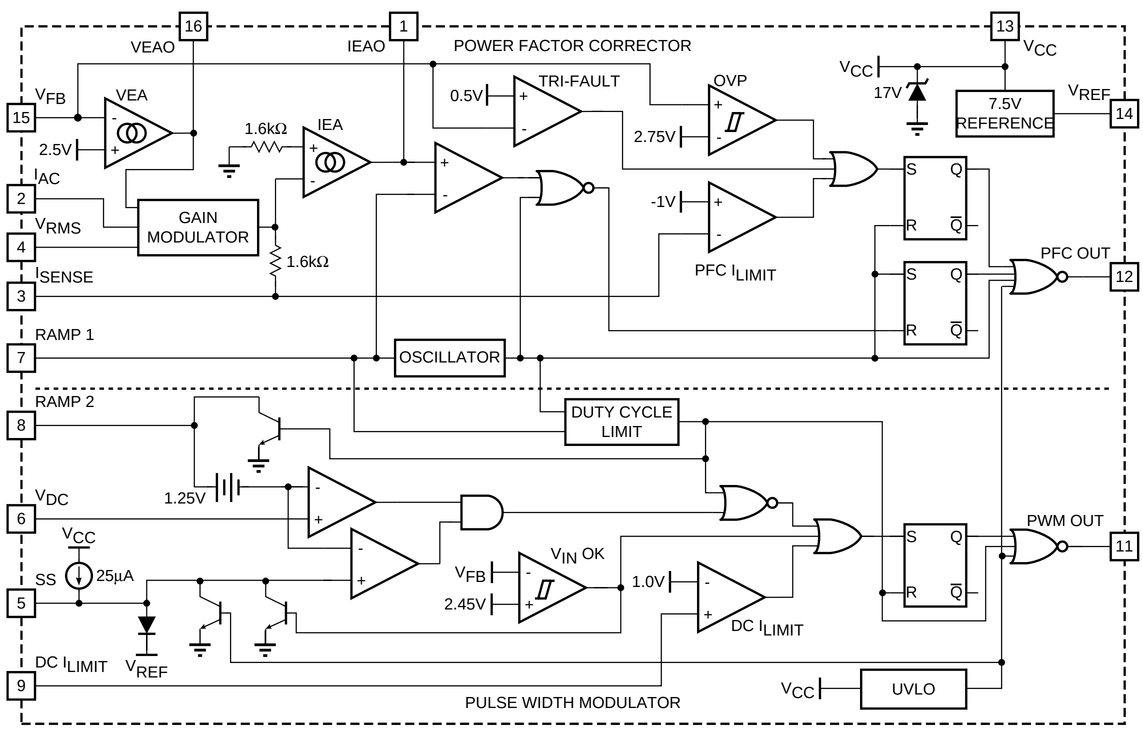
- Internally synchronized leading-edge PFC and trailing-edge PWM in one IC
- TriFault Detect™ for UL1950 compliance and enhanced safety
- Slew rate enhanced transconductance error amplifier for ultra-fast PFC response
- Low power: 200µA startup current, 5.5mA operating current
- Low total harmonic distortion, high PF
- Reduced ripple current in storage capacitor between PFC and PWM sections
- Average current, continuous boost leading edge PFC
- PWM configurable for current-mode or voltage mode operation
- Current fed gain modulator for improved noise immunity
- Overvoltage and brown-out protection, UVLO, and soft start

General Description

The ML4800 is a controller for power factor corrected, switched mode power supplies. Power Factor Correction (PFC) allows the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply that fully complies with IEC1000-3-2 specification. Intended as a BiCMOS version of the industry-standard ML4824, the ML4800 includes circuits for the implementation of leading edge, average current, “boost” type power factor correction and a trailing edge, pulse width modulator (PWM). It also includes a TriFault Detect™ function to help ensure that no unsafe conditions will result from single component failure in the PFC. Gate-drivers with 1A capabilities minimize the need for external driver circuits. Low power requirements improve efficiency and reduce component costs.

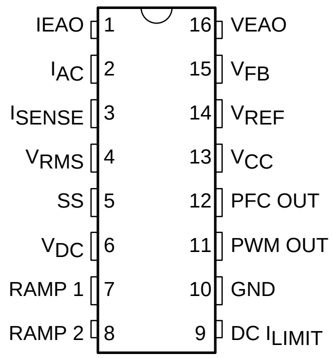
An over-voltage comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and input voltage brownout protection. The PWM section can be operated in current or voltage mode, at up to 250kHz, and includes an accurate 50% duty cycle limit to prevent transformer saturation.

Block Diagram



Pin Configuration

ML4800
16-Pin PDIP (P16)
16-Pin Narrow SOIC (S16N)



TOP VIEW

Pin Description

Pin	Name	Function
1	IEAO	Slew rate enhanced PFC transconductance error amplifier output
2	I_{AC}	PFC AC line reference input to Gain Modulator
3	I_{SENSE}	Current sense input to the PFC Gain Modulator
4	V_{RMS}	PFC Gain Modulator RMS line voltage compensation input
5	SS	Connection point for the PWM soft start capacitor
6	V_{DC}	PWM voltage feedback input
7	RAMP 1	Oscillator timing node; timing set by R_TC_T
8	RAMP 2	When in current mode, this pin functions as the current sense input; when in voltage mode, it is the PWM modulation ramp input.
9	DC I_{LIMIT}	PWM cycle-by-cycle current limit comparator input
10	GND	Ground
11	PWM OUT	PWM driver output
12	PFC OUT	PFC driver output
13	V_{CC}	Positive supply
14	V_{REF}	Buffered output for the internal 7.5V reference
15	V_{FB}	PFC transconductance voltage error amplifier input
16	VEAO	PFC transconductance voltage error amplifier output

Abolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min.	Max.	Units
V_{CC}		18	V
I_{SENSE} Voltage	-5	0.7	V
Voltage on Any Other Pin	GND - 0.3	V_{CCZ} + 0.3	V
I_{REF}		10	mA
I_{AC} Input Current		10	mA
Peak PFC OUT Current, Source or Sink		1	A
Peak PWM OUT Current, Source or Sink		1	A
PFC OUT, PWM OUT Energy Per Cycle		1.5	µJ
Junction Temperature		150	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10 sec)		260	°C
Thermal Resistance (θ_{JA}) Plastic DIP Plastic SOIC		 80 105	 °C/W °C/W

Operating Conditions

Temperature Range	Min	.Max.	Units
ML4800CX	0	70	°C
ML4800IX	-40	85	°C

Electrical Characteristics

Unless otherwise specified, V_{CC} = 15V, R_T = 52.3kΩ, C_T = 470pF, T_A = Operating Temperature Range (Note 1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Error Amplifier						
	Input Voltage Range		0		5	V
	Transconductance	$V_{NON\ INV} = V_{INV}$, VEAO = 3.75V	30	65	90	µ℧
	Feedback Reference Voltage		2.43	2.5	2.57	V
	Input Bias Current	Note 2		-0.5	-1.0	µA
	Output High Voltage		6.0	6.7		V
	Output Low Voltage			0.1	0.4	V
	Source Current	$V_{IN} = \pm 0.5V$, $V_{OUT} = 6V$	-40	-140		µA
	Sink Current	$V_{IN} = \pm 0.5V$, $V_{OUT} = 1.5V$	40	140		µA
	Open Loop Gain		50	60		dB
	Power Supply Rejection Ratio	$11V < V_{CC} < 16.5V$	50	60		dB
Current Error Amplifier						
	Input Voltage Range		-1.5		2	V
	Transconductance	$V_{NON\ INV} = V_{INV}$, VEAO = 3.75V	50	100	150	µ℧
	Input Offset Voltage		0	4	15	mV

Electrical Characteristics (Continued)

Unless otherwise specified, V_{CC} = 15V, R_T = 52.3kΩ, C_T = 470pF, T_A = Operating Temperature Range (Note 1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	Input Bias Current			-0.5	-1.0	µA
	Output High Voltage		6.0	6.7		V
	Output Low Voltage			0.65	1.0	V
	Source Current	V_{IN} = ±0.5V, V_{OUT} = 6V	-40	-104		µA
	Sink Current	V_{IN} = ±0.5V, V_{OUT} = 1.5V	40	160		µA
	Open Loop Gain		60	70		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	60	75		dB
OVP Comparator						
	Threshold Voltage		2.65	2.75	2.85	V
	Hysteresis		175	250	325	mV
Tri-Fault Detect						
	Fault Detect HIGH		2.65	2.75	2.85	V
	Time to Fault Detect HIGH	V_{FB} = $V_{FAULT\ DETECT\ LOW}$ to V_{FB} = OPEN. 470pF from V_{FB} to GND		2	4	ms
	Fault Detect LOW		0.4	0.5	0.6	V
PFC I_{LIMIT} Comparator						
	Threshold Voltage		-0.9	-1.0	-1.1	V
	(PFC I_{LIMIT} V_{TH} - Gain Modulator Output)		120	220		mV
	Delay to Output			150	300	ns
DC I_{LIMIT} Comparator						
	Threshold Voltage		0.95	1.0	1.05	V
	Input Bias Current			±0.3	±1	µA
	Delay to Output			150	300	ns
V_{IN} OK Comparator						
	Threshold Voltage		2.35	2.45	2.55	V
	Hysteresis		0.8	1.0	1.2	V
GAIN Modulator						
	Gain (Note 3)	I_{AC} = 100µA, V_{RMS} = V_{FB} = 0V	0.60	0.80	1.05	
		I_{AC} = 50µA, V_{RMS} = 1.2V, V_{FB} = 0V	1.8	2.0	2.40	
		I_{AC} = 50µA, V_{RMS} = 1.8V, V_{FB} = 0V	0.85	1.0	1.25	
		I_{AC} = 100µA, V_{RMS} = 3.3V, V_{FB} = 0V	0.20	0.30	0.40	
	Bandwidth	I_{AC} = 100µA		10		MHz
	Output Voltage	I_{AC} = 350µA, V_{RMS} = 1V, V_{FB} = 0V	0.60	0.75	0.9	V
Oscillator						
	Initial Accuracy	T_A = 25°C	71	76	81	kHz
	Voltage Stability	11V < V_{CC} < 16.5V		1		%
	Temperature Stability			2		%
	Total Variation	Line, Temp	68		84	kHz
	Ramp Valley to Peak Voltage			2.5		V

Electrical Characteristics (Continued)

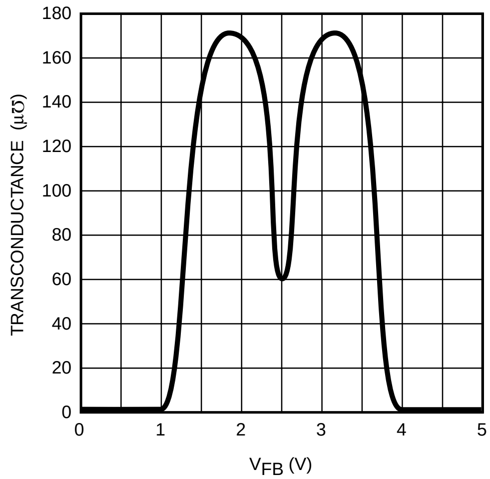
Unless otherwise specified, V_{CC} = 15V, R_T = 52.3kΩ, C_T = 470pF, T_A = Operating Temperature Range (Note 1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	PFC Dead Time		350		650	ns
	C_T Discharge Current	$V_{RAMP\ 2}$ = 0V, $V_{RAMP\ 1}$ = 2.5V	3.5	5.5	7.5	mA
Reference						
	Output Voltage	T_A = 25°C, I(V_{REF}) = 1mA	7.4	7.5	7.6	V
	Line Regulation	11V <V_{CC} <16.5V		10	25	mV
	Load Regulation	0mA <I(V_{REF}) < 10mA; T_A = 0°C to 70°C		10	20	mV
		0mA < I(V_{REF}) < 5mA; T_A = –40°C to 85°C		10	20	mV
	Temperature Stability			0.4		%
	Total Variation	Line, Load, Temp	7.35		7.65	V
	Long Term Stability	T_J = 125°C, 1000 Hours		5	25	mV
PFC						
	Minimum Duty Cycle	V_{IEAO} > 4.0V			0	%
	Maximum Duty Cycle	V_{IEAO} < 1.2V	90	95		%
	Output Low Voltage	I_{OUT} = -20mA		0.4	0.8	V
		I_{OUT} = -100mA		0.7	2.0	V
		I_{OUT} = 10mA, V_{CC} = 9V		0.4	0.8	V
	Output High Voltage	I_{OUT} = 20mA	V_{CC} - 0.8V			V
		I_{OUT} = 100mA	V_{CC} - 2V			V
	Rise/Fall Time	C_L = 1000pF		50		ns
PWM						
	Duty Cycle Range		0-44	0-47	0-49	%
	Output Low Voltage	I_{OUT} = -20mA		0.4	0.8	V
		I_{OUT} = -100mA		0.7	2.0	V
		I_{OUT} = 10mA, V_{CC} = 9V		0.4	0.8	V
	Output High Voltage	I_{OUT} = 20mA	V_{CC} - 0.8V			V
		I_{OUT} = 100mA	V_{CC} - 2V			V
	Rise/Fall Time	C_L = 1000pF		50		ns
Supply						
	Start-up Current	V_{CC} = 12V, C_L = 0		200	350	µA
	Operating Current	14V, C_L = 0		5.5	7	mA
	Undervoltage Lockout Threshold		12.4	13	13.6	V
	Undervoltage Lockout Hysteresis		2.5	2.8	3.1	V

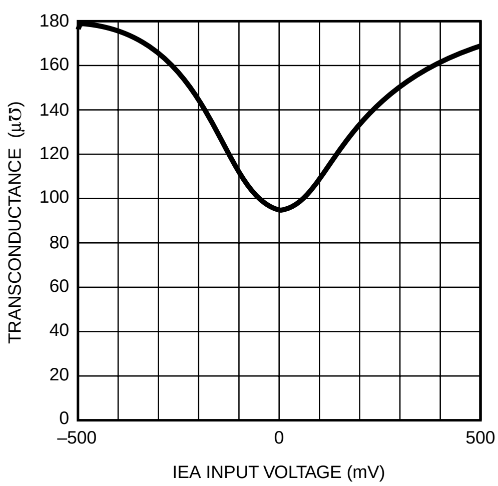
Notes

1. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
2. Includes all bias currents to other circuits connected to the V_{FB} pin.
3. Gain = K x 5.3V; K = ($I_{GAINMOD}$ - I_{OFFSET}) x [I_{AC} (VEAO - 0.625)]$^{-1}$; $VEAO_{MAX}$=5V.

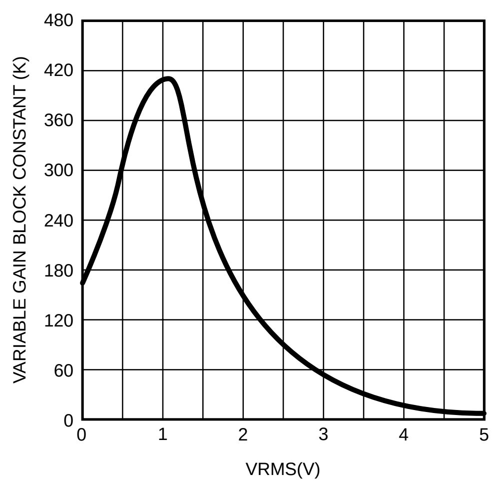
Typical Performance Characteristics



Voltage Error Amplifier (VEA) Transconductance (g_m)



Current Error Amplifier (IEA) Transconductance (g_m)



Gain Modulator Transfer Characteristic (K)

$$K = \frac{(I_{GAINMOD} - 84\mu A)}{IAC \times (5 - 0.625)} mV^{-1}$$

Functional Description

The ML4800 consists of an average current controlled, continuous boost Power Factor Corrector (PFC) front end and a synchronized Pulse Width Modulator (PWM) back end. The PWM can be used in either current or voltage mode. In voltage mode, feedforward from the PFC output buss can be used to improve the PWM's line regulation. In either mode, the PWM stage uses conventional trailing-edge duty cycle modulation, while the PFC uses leading-edge modulation. This patented leading/trailing edge modulation technique results in a higher usable PFC error amplifier bandwidth, and can significantly reduce the size of the PFC DC buss capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). The PWM section of the ML4800 runs at the same frequency as the PFC.

In addition to power factor correction, a number of protection features have been built into the ML4800. These include soft-start, PFC overvoltage protection, peak current limiting, brownout protection, duty cycle limiting, and under-voltage lockout.

Power Factor Correction

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect, which occurs on the input filter capacitor in these supplies, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current inphase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the ML4800 uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current drawn from the power line is proportional to the input line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of $270VAC_{rms}$. The other condition is that the current drawn from the line at any given instant must be proportional to the line voltage. Establishing a suitable voltage control loop for the converter, which in turn drives a current error amplifier and switching output driver satisfies the first of these requirements. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current that varies directly with the input voltage. In order to prevent ripple, which will necessarily appear at the output of the boost circuit (typically about 10VAC on a 385V DC level), from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC such to be proportional to $1/V_{IN}2$, which linearizes the transfer function of the system as the AC input voltage varies.

Since the boost converter topology in the ML4800 PFC is of the current-averaging type, no slope compensation is required.

PFC Section

Gain Modulator

Figure 1 shows a block diagram of the PFC section of the ML4800. The gain modulator is the heart of the PFC, as it is this circuit block which controls the response of the current loop to line voltage waveform and frequency, rms line voltage, and PFC output voltage. There are three inputs to the gain modulator. These are:

1. A current representing the instantaneous input voltage (amplitude and waveshape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at I_{AC}. Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.

2. A voltage proportional to the long-term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at V_{RMS}. The gain modulator s output is inversely proportional to $V_{RMS}{}^2$ (except at unusually low values of V_{RMS} where special gain contouring takes over, to limit power dissipation of the circuit components under heavy brownout conditions). The relationship between V_{RMS} and gain is called K, and is illustrated in the Typical Performance Characteristics.

3. The output of the voltage error amplifier, VEAO. The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual-ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC from the power line. The general form for the output of the gain modulator is:

$$I_{GAINMOD} = \frac{I_{AC} \times VEAO}{V_{RMS}^2} \times 1V \qquad (1)$$

More exactly, the output current of the gain modulator is given by:

$$I_{GAINMOD} = K \times (VEAO - 0.625V) \times I_{AC}$$

where K is in units of V^{-1}.

Note that the output current of the gain modulator is limited to 500µA.

Current Error Amplifier

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the I_{SENSE} pin. The negative voltage on I_{SENSE} represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier. In higher power applications, two current transformers are sometimes used, one to monitor the ID of the boost MOSFET(s) and one to monitor the I_F of the boost diode. As stated above, the inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on I_{SENSE} is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease, to achieve a less negative voltage on the I_{SENSE} pin.

Cycle-By-Cycle Current Limiter

The I_{SENSE} pin, as well as being a part of the current feedback loop, is a direct input to the cycle-by-cycle current limiter for the PFC section. Should the input voltage at this pin ever be more negative than -1V, the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

TriFault Detect™

To improve power supply reliability, reduce system component count, and simplify compliance to UL 1950 safety standards, the ML4800 includes TriFault Detect. This feature monitors VFB (Pin 15) for certain PFC fault conditions.

In the case of a feedback path failure, the output of the PFC could go out of safe operating limits. With such a failure, VFB will go outside of its normal operating area. Should VFB go too low, too high, or open, TriFault Detect senses the error and terminates the PFC output drive.

TriFault detect is an entirely internal circuit. It requires no external components to serve its protective function.

Overvoltage Protection

The OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should suddenly change. A resistor divider from the high voltage DC output of the PFC is fed to V_{FB}. When the voltage on V_{FB} exceeds 2.75V, the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has 250mV of hysteresis, and the PFC will not restart until the voltage at V_{FB} drops below 2.50V. The V_{FB} should be set at a level where the active and passive external power components and the ML4800 are within their safe operating voltages, but not so low as to interfere with the boost voltage regulation loop.

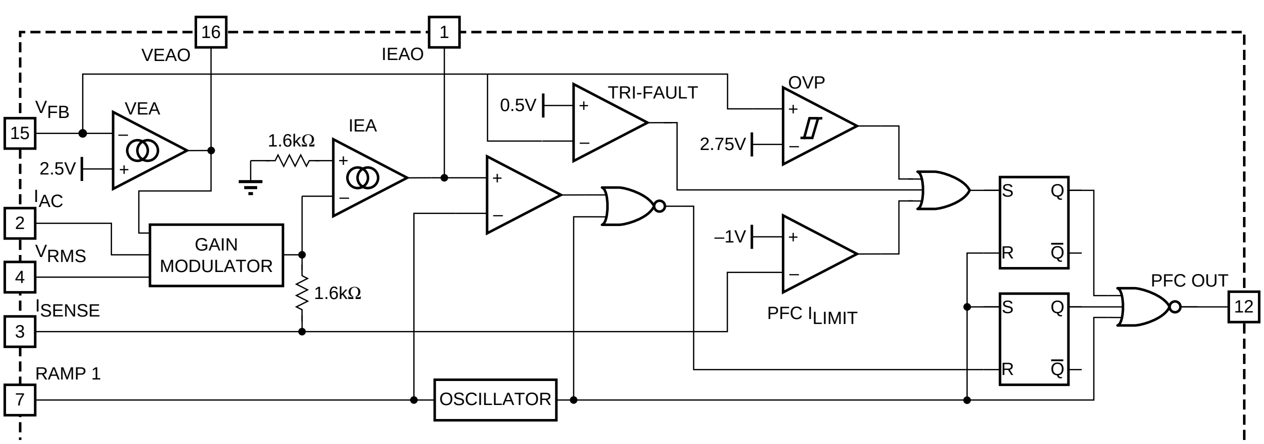


Figure 1. PFC Section Block Diagram

Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 2 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to V_{REF} to produce a soft-start characteristic on the PFC: as the reference voltage comes up from zero volts, it creates a differentiated voltage on IEAO which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

There are two major concerns when compensating the voltage loop error amplifier; stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open-loop crossover frequency should be 1/2 that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency). The gain vs. input voltage of the ML4800's voltage error amplifier has a specially shaped non-linearity such that under steady-state operating conditions the transconductance of the error amplifier is at a local minimum. Rapid perturbations in line or load conditions will cause the input to the voltage error amplifier (V_{FB}) to deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier will increase significantly, as shown in the Typical Performance Characteristics. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with a conventional linear gain characteristic.

The current amplifier compensation is similar to that of the voltage error amplifier with the exception of the choice of crossover frequency. The crossover frequency of the current amplifier should be at least 10 times that of the voltage amplifier, to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency, e.g. 16.7kHz for a 100kHz switching frequency.

There is a modest degree of gain contouring applied to the transfer characteristic of the current error amplifier, to increase its speed of response to current-loop perturbations. However, the boost inductor will usually be the dominant factor in overall current loop response. Therefore, this contouring is significantly less marked than that of the voltage error amplifier. This is illustrated in the Typical Performance Characteristics.

For more information on compensating the current and voltage control loops, see Application Notes 33 and 34. Application Note 16 also contains valuable information for the design of this class of PFC.

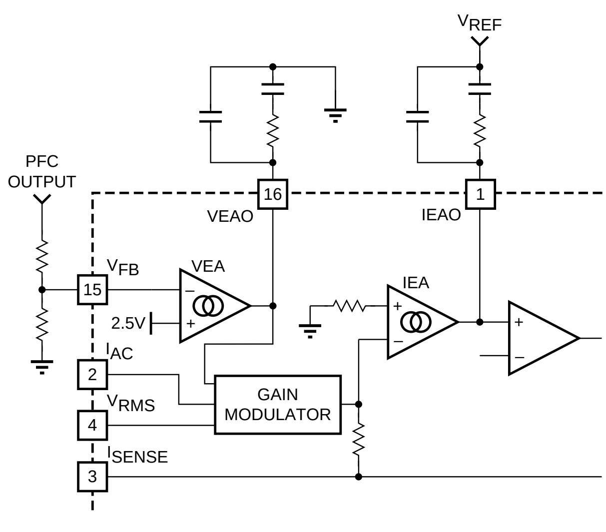


Figure 2. Compensation Network Connections for the Voltage and Current Error Amplifiers

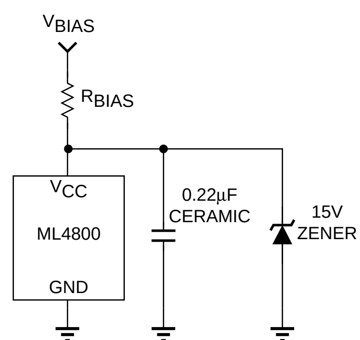


Figure 3. External Component Connections to V_{CC}

Oscillator (RAMP 1)

The oscillator frequency is determined by the values of R_T and C_T, which determine the ramp and off-time of the oscillator output clock:

$$f_{OSC} = \frac{1}{t_{RAMP} + t_{DEADTIME}} \quad (2)$$

The dead time of the oscillator is derived from the following equation:

$$t_{RAMP} = C_T \times R_T \times \ln\frac{V_{REF} - 1.25}{V_{REF} - 3.75} \quad (3)$$

at V_{REF} = 7.5V:

$$t_{RAMP} = C_T \times R_T \times 0.51$$

The dead time of the oscillator may be determined using:

$$t_{DEADTIME} = \frac{2.5V}{5.5mA} \times C_T = 450 \times C_T \quad (4)$$

The dead time is so small (tRAMP >> $t_{DEADTIME}$) that the operating frequency can typically be approximated by:

$$f_{OSC} = \frac{1}{t_{RAMP}} \quad (5)$$

EXAMPLE:
For the application circuit shown in the data sheet, with the oscillator running at:

$$f_{OSC} = 100kHz = \frac{1}{t_{RAMP}}$$

Solving for R_T x C_T yields 1.96 x 10^{-4}. Selecting standard components values, C_T = 390pF, and R_T = 51.1kΩ.

The dead time of the oscillator adds to the Maximum PWM Duty Cycle (it is an input to the Duty Cycle Limiter). With zero oscillator dead time, the Maximum PWM Duty Cycle is typically 45%. In many applications, care should be taken that C_T not be made so large as to extend the Maximum Duty Cycle beyond 50%. This can be accomplished by using a stable 390pF capacitor for C_T.

PWM SECTION

Pulse Width Modulator

The PWM section of the ML4800 is straightforward, but there are several points which should be noted. Foremost among these is its inherent synchronization to the PFC section of the device, from which it also derives its basic timing. The PWM is capable of current-mode or voltage mode operation. In current-mode applications, the PWM ramp (RAMP 2) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage, and is thereby representative of the current flowing in the converter's output stage. DC I_{LIMIT}, which provides cycle-by-cycle current limiting, is typically connected to RAMP 2 in such applications. For voltage-mode operation or certain specialized applications, RAMP 2 can be connected to a separate RC timing network to generate a voltage ramp against which V_{DC} will be compared. Under these conditions, the use of voltage feedforward from the PFC buss can assist in line regulation accuracy and response. As in current mode operation, the DC I_{LIMIT} input is used for output stage overcurrent protection.

No voltage error amplifier is included in the PWM stage of the ML4800, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of optocoupler feedback circuitry, an offset has been built into the PWM's RAMP 2 input which allows V_{DC} to command a zero percent duty cycle for input voltages below 1.25V.

PWM Current Limit

The DC I_{LIMIT} pin is a direct input to the cycle-by-cycle current limiter for the PWM section. Should the input voltage at this pin ever exceed 1V, the output of the PWM will be disabled until the output flip-flop is reset by the clock pulse at the start of the next PWM power cycle.

V_{IN} OK Comparator

The V_{IN} OK comparator monitors the DC output of the PFC and inhibits the PWM if this voltage on V_{FB} is less than its nominal 2.45V. Once this voltage reaches 2.45V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, the soft-start begins.

PWM Control (RAMP 2)

When the PWM section is used in current mode, RAMP 2 is generally used as the sampling point for a voltage representing the current in the primary of the PWM's output transformer, derived either by a current sensing resistor or a current transformer. In voltage mode, it is the input for a ramp voltage generated by a second set of timing components (R_{RAMP2}, C_{RAMP2}), that will have a minimum value of zero volts and should have a peak value of approximately 5V. In voltage mode operation, feedforward from the PFC output buss is an excellent way to derive the timing ramp for the PWM stage.

Soft Start

Start-up of the PWM is controlled by the selection of the external capacitor at SS. A current source of 25µA supplies the charging current for the capacitor, and start-up of the PWM begins at 1.25V. Start-up delay can be programmed by the following equation:

$$C_{SS} = t_{DELAY} \times \frac{25\mu A}{1.25V} \quad (6)$$

where C_{SS} is the required soft start capacitance, and t_{DELAY} is the desired start-up delay.

It is important that the time constant of the PWM soft-start allow the PFC time to generate sufficient output power for the PWM section. The PWM start-up delay should be at least 5ms.

Solving for the minimum value of C_{SS}:

$$Css = 5ms \times \frac{25\mu A}{1.25V} = 100nF \quad (6a)$$

Caution should be exercised when using this minimum soft start capacitance value because premature charging of the SS capacitor and activation of the PWM section can result if V_{FB} is in the hysteresis band of the V_{IN} OK comparator at start-up. The magnitude of V_{FB} at start-up is related both to line voltage and nominal PFC output voltage. Typically, a 1.0µF soft start capacitor will allow time for V_{FB} and PFC out to reach their nominal values prior to activation of the PWM section at line voltages between 90Vrms and 265Vrms.

Generating V_{CC}

The ML4800 is a voltage-fed part. It requires an external 15V, ±10% (or better) shunt voltage regulator, or some other V_{CC} regulator, to regulate the voltage supplied to the part at 15V nominal. This allows low power dissipation while at the same time delivering 13V nominal gate drive at the PWM OUT and PFC OUT outputs. If using a Zener diode for this function, it is important to limit the current through the Zener to avoid overheating or destroying it. This can be easily done with a single resistor in series with the Vcc pin, returned to a bias supply of typically 18V to 20V. The resistor's value must be chosen to meet the operating current requirement of the ML4800 itself (8.5mA, max.) plus the current required by the two gate driver outputs.

EXAMPLE:
With a V_{BIAS} of 20V, a V_{CC} of 15V and the ML4800 driving a total gate charge of 90nC at 100kHz (e.g., 1 IRF840 MOSFET and 2 IRF820 MOSFETs), the gate driver current required is:

$$I_{GATEDRIVE} = 100kHz \times 90nC = 9mA \quad (7)$$

$$R_{BIAS} = \frac{V_{BIAS} - V_{CC}}{I_{CC} + I_G + I_Z} \quad (8)$$

$$R_{BIAS} = \frac{20V - 15V}{6mA + 9mA + 5mA} = 250\Omega$$

Choose R_{BIAS} = 240Ω.

The ML4800 should be locally bypassed with a 1.0µF ceramic capacitor. In most applications, an electrolytic capacitor of between 47µF and 220µF is also required across the part, both for filtering and as part of the start-up bootstrap circuitry.

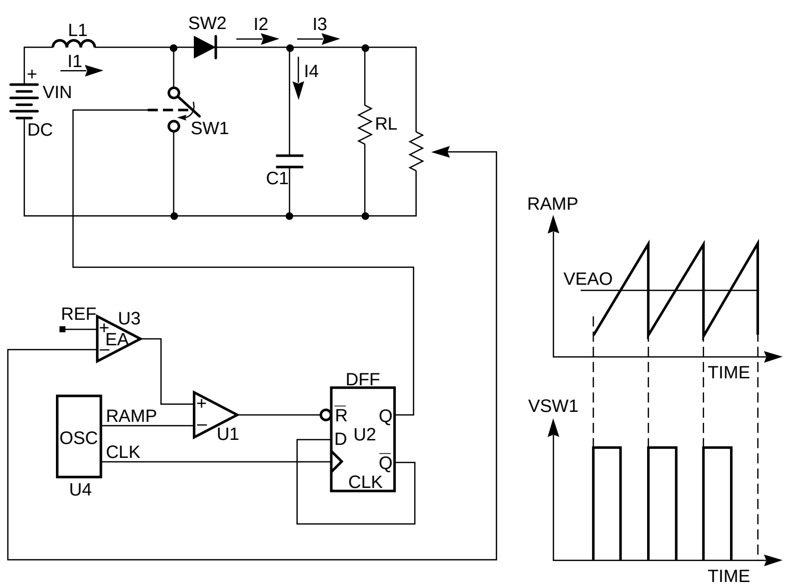


Figure 4. Typical Trailing Edge Control Scheme

Leading/Trailing Modulation

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. The error amplifier output voltage is then compared with the modulating ramp. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 4 shows a typical trailing edge control scheme.

In the case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during the OFF time of the switch. Figure 5 shows a leading edge control scheme.

One of the advantages of this control technique is that it requires only one system clock. Switch 1 (SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary “no-load” period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC’s output ripple voltage can be reduced by as much as 30% using this method.

Typical Applications

Figure 6 is the application circuit for a complete 100W power factor corrected power supply, designed using the methods and general topology detailed in Application Note 33.

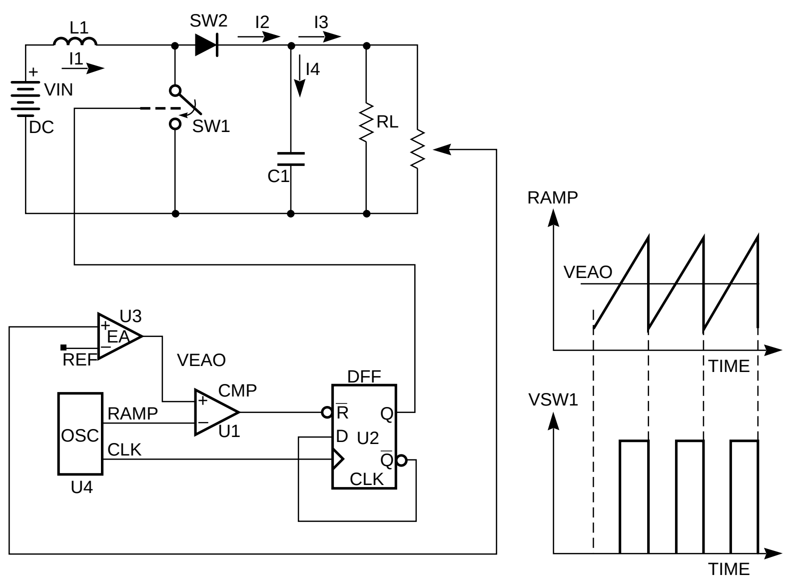


Figure 5. Typical Leading Edge Control Scheme

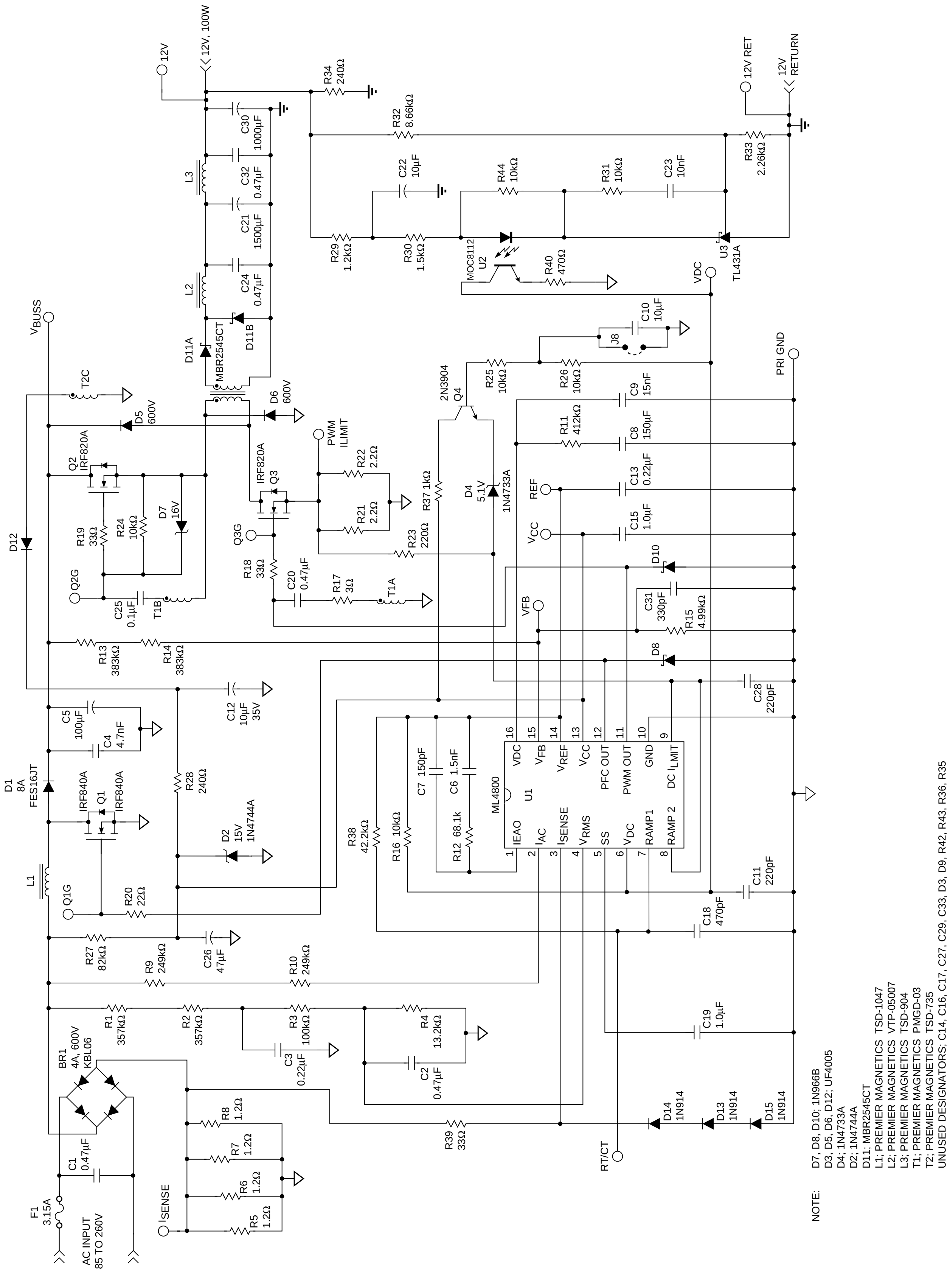


Figure 6. 100W Power Factor Corrected Power Supply, Designed Using Micro Linear Application Note 33

Ordering Information

Part Number	Temperature Range	Package
ML4800CP	0°C to 70°C	16-Pin PDIP (P16)
ML4800CS	0°C to 70°C	16-Pin Narrow SOIC (S16N)
ML4800IP	-40°C to 85°C	16-Pin PDIP (P16)
ML4800IS	-40°C to 85°C	16-Pin Narrow SOIC (S16N)

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Stock#DS30004800